DOE Office of Electricity TRAC

Peer Review

U.S. DEPARTMENT OF ENERGY | OFFICE OF ELECTRICITY

Intelligent Power Stage

PRINCIPAL INVESTIGATORS

Dr. Alex Q. Huang, Professor, The University of Texas at Austin

PROJECT TEAM

Dr. Ruiyang Yu, Research Scientist, The University of Texas at Austin

Zibo Chen, Research Assistant, The University of Texas at Austin

Houshang Salimian, Research Assistant, The University of Texas at Austin

Chen Chen, Research Assistant, The University of Texas at Austin

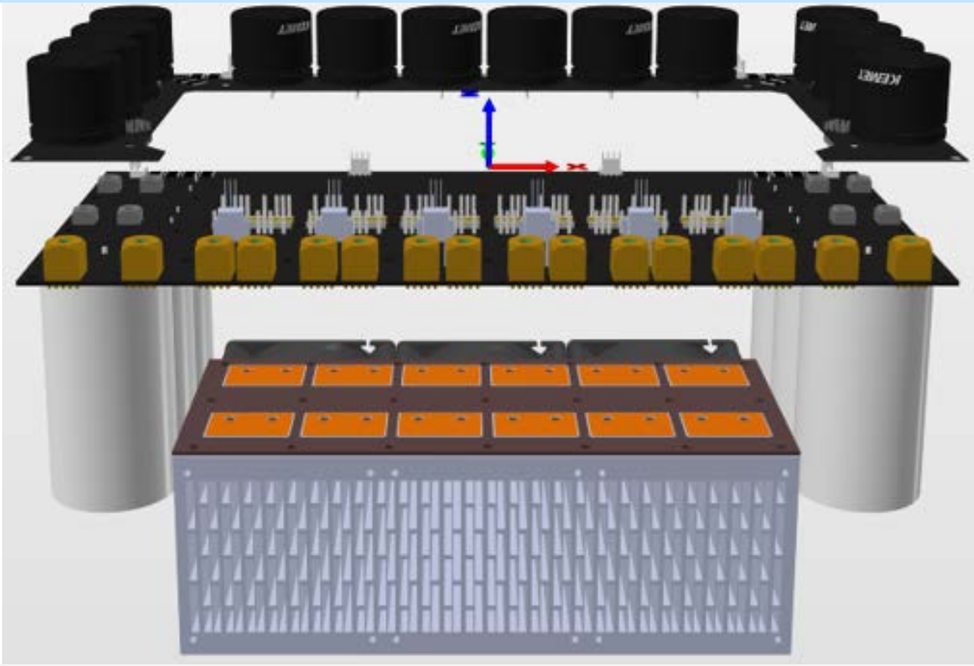
Rahul Choudhary, Research Assistant, The University of Texas at Austin

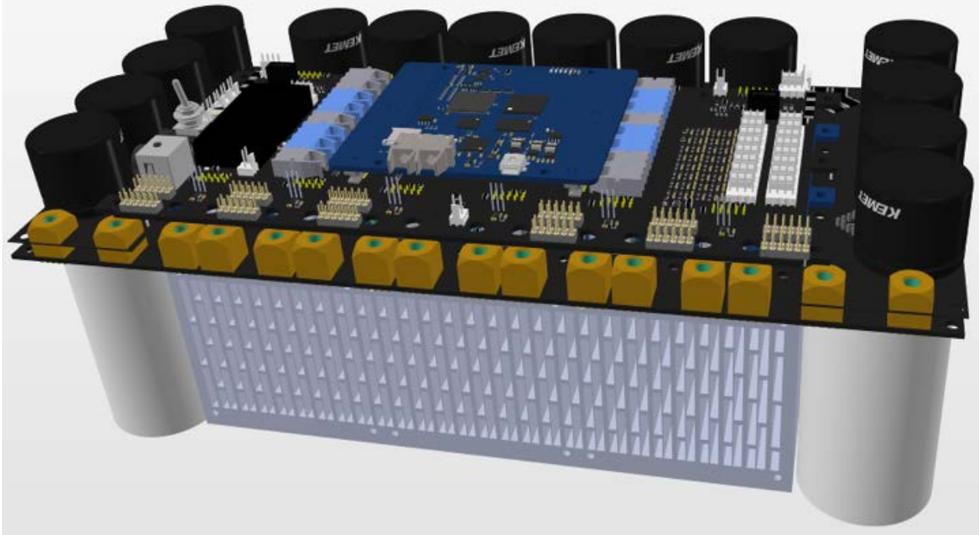
PROJECT SUMMARY

To design, develop and validate a high power and high density intelligent power stage (IPS) for bidirectional DC/AC applications with standardized power ports and communication ports to allow maximum flexibility to operate with other similar IPS and to interface with an external controller.

Innovations

- 1. High density and low cost SiC IPS
- 2. Advanced packaging with improved thermal management
- 3. Intelligent gate driving, Von and T online measurement, over current protection
- 4. Self-contained auxiliary power supply unit
- 5. Advanced DSP+FPGA controller and communication with external SUPER controller
- 6. Multiple grid functions (Black start, LVRT)

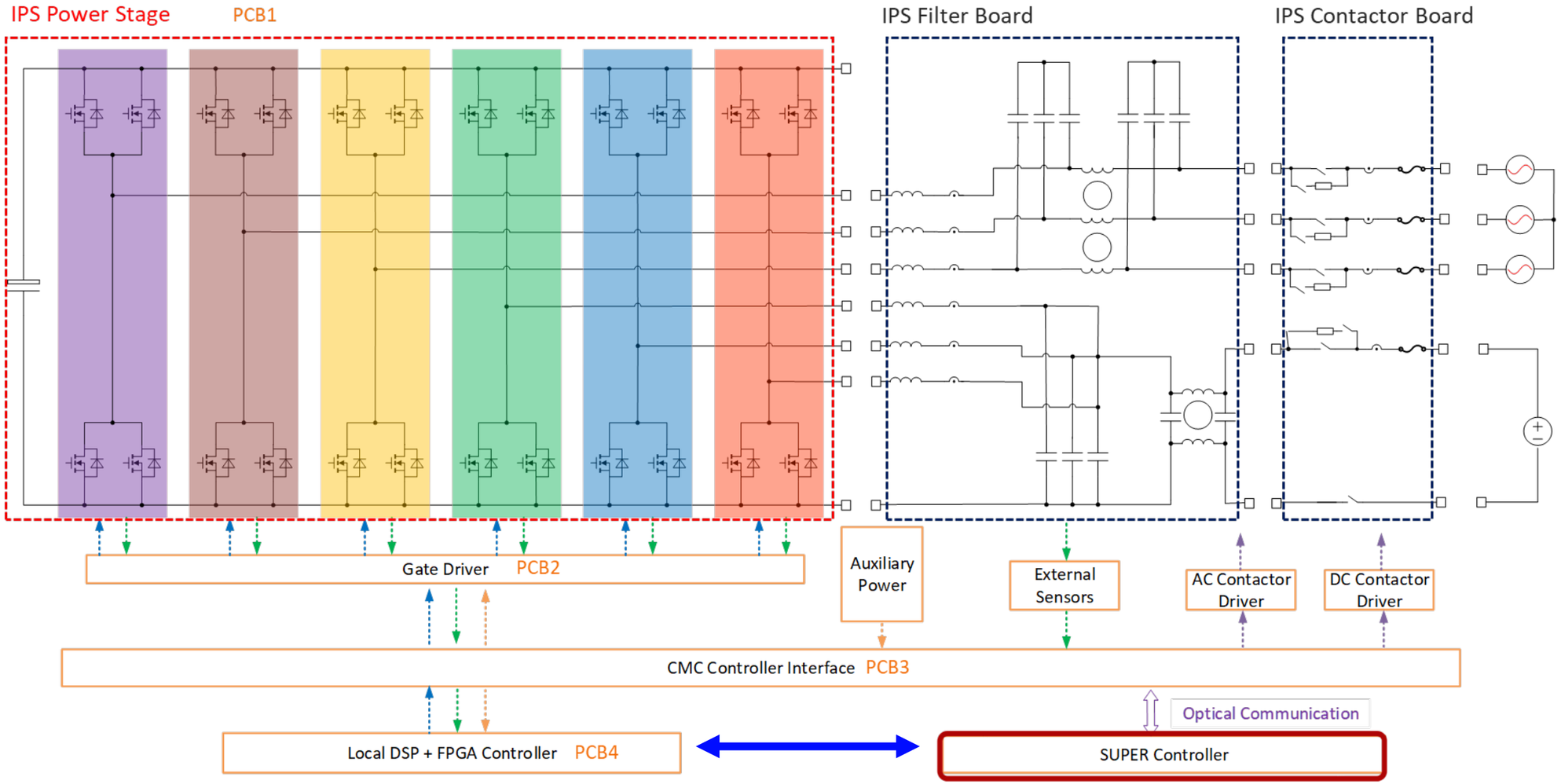




Innovation Update

1. High density and low cost system level SiC IPS packaging

UT SPEC SiC IPS Architecture

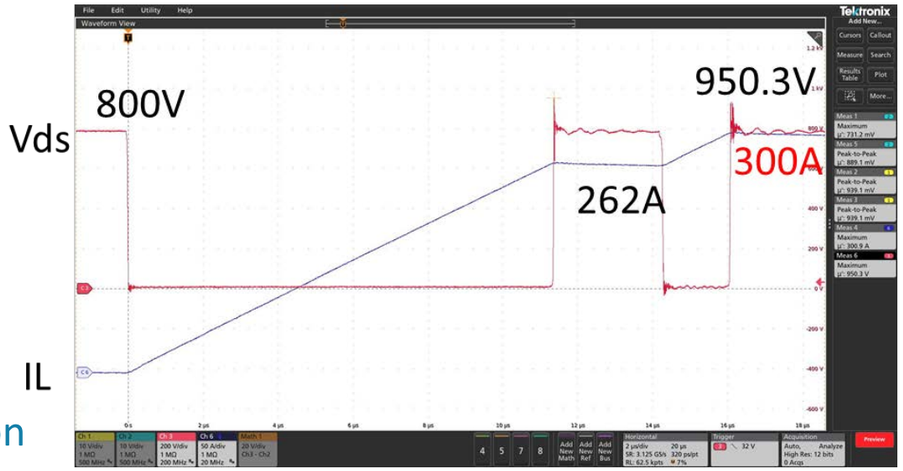


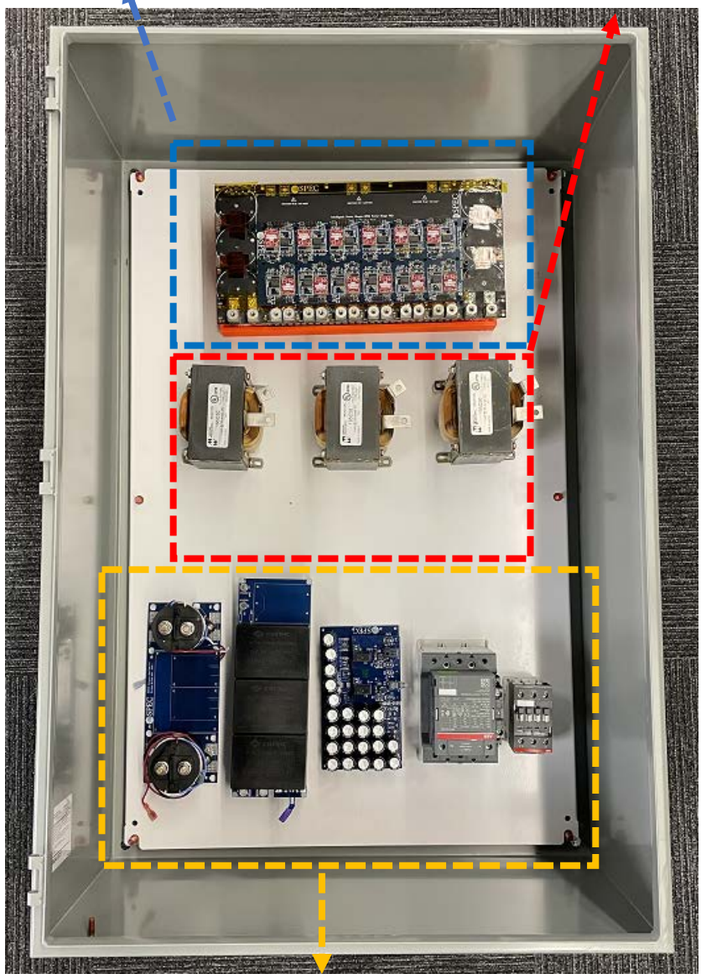
Innovation Update

1. High density and low cost system level SiC IPS packaging

Power: >75kVA
Switching Frequency: 30 kHz
Configuration: Six Phase Legs
Dimension: 345mm*165mm*120mm
Weight: 5.5 kg
Power stage power density: 11 kW/L
Estimated Cost: $86/kVA

- SiC FET + DBC + baseplate module
- Heatsink + Fans + DC capacitor
- Gate driver for parallel device
- DSP + FPGA controller
- On board sensors:
- 12 temperature, 6 current, and 2 voltage
- 16 ADC and 16 Fiber for remote connection



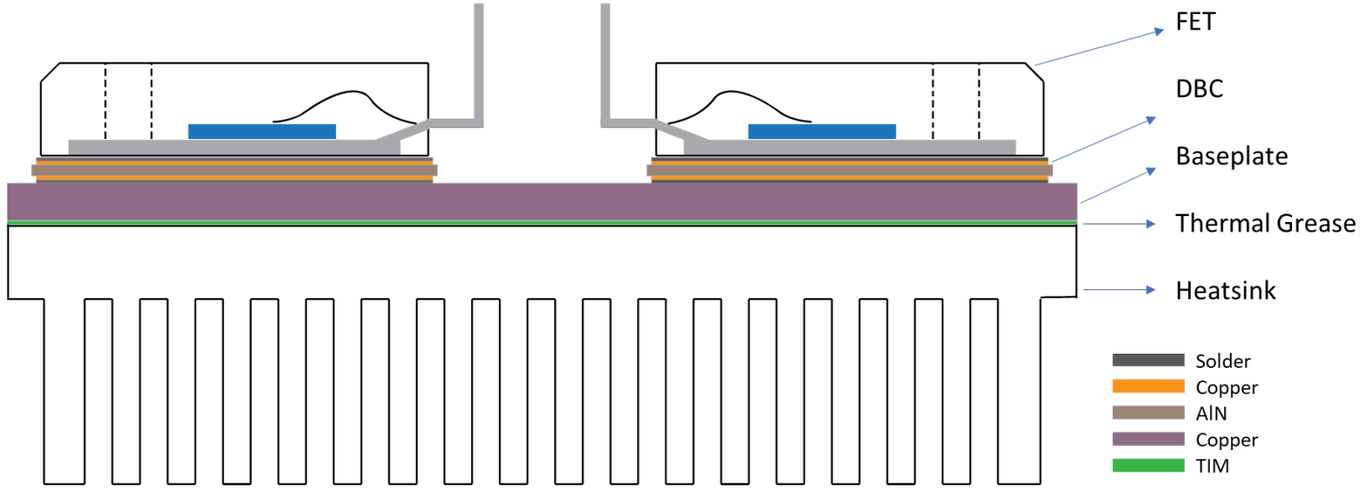


Innovation Update

2. Advanced thermal management and cooling technology

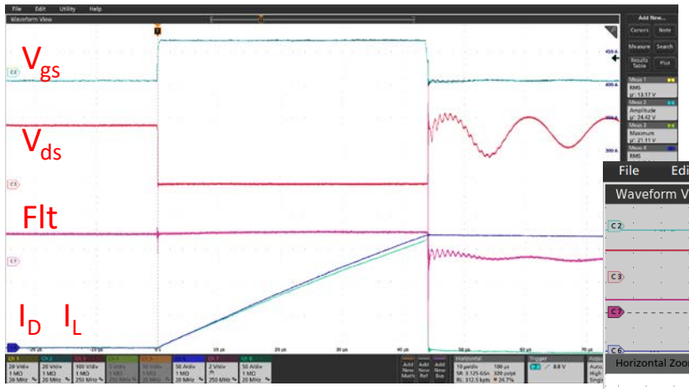
.

- Innovative 24-switch SiC modules based on high performance and low cost cascode SiC FET, DBC and base plate.
- Controlled fan speed for system loss optimization and noise reduction.
- Verified >2kW power loss dissipation capability.
  - The extracted R_{ja} is about 1°C/W per switch.



Innovation Update

3. Intelligent gate driving, V_{on} and T measurement, over current (OC) protection



OC Protection at 170A, soft turn-off in 400ns

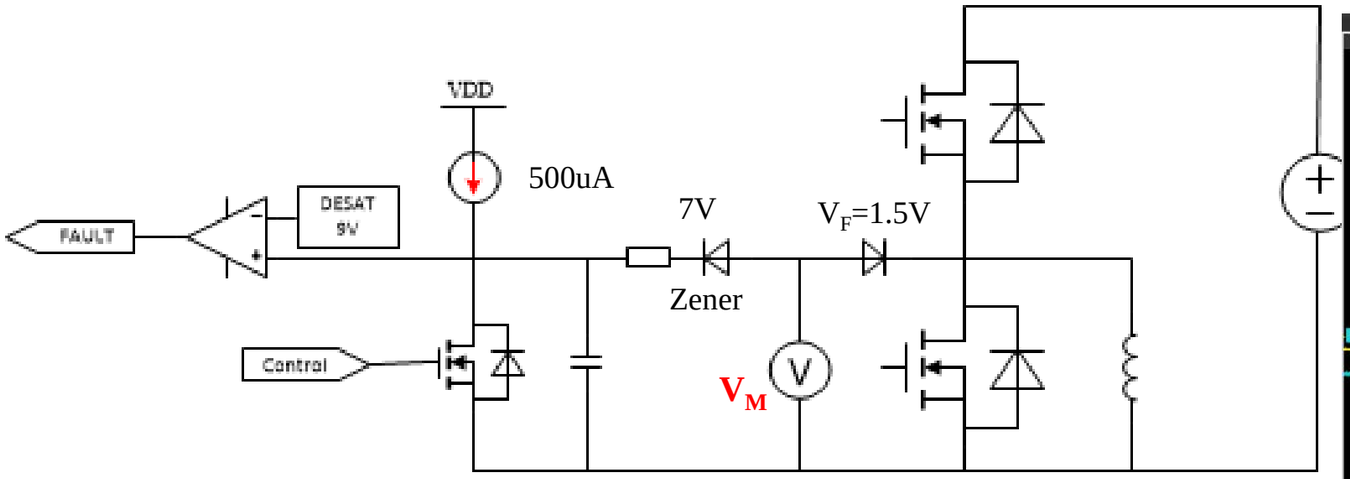
Innovation Update

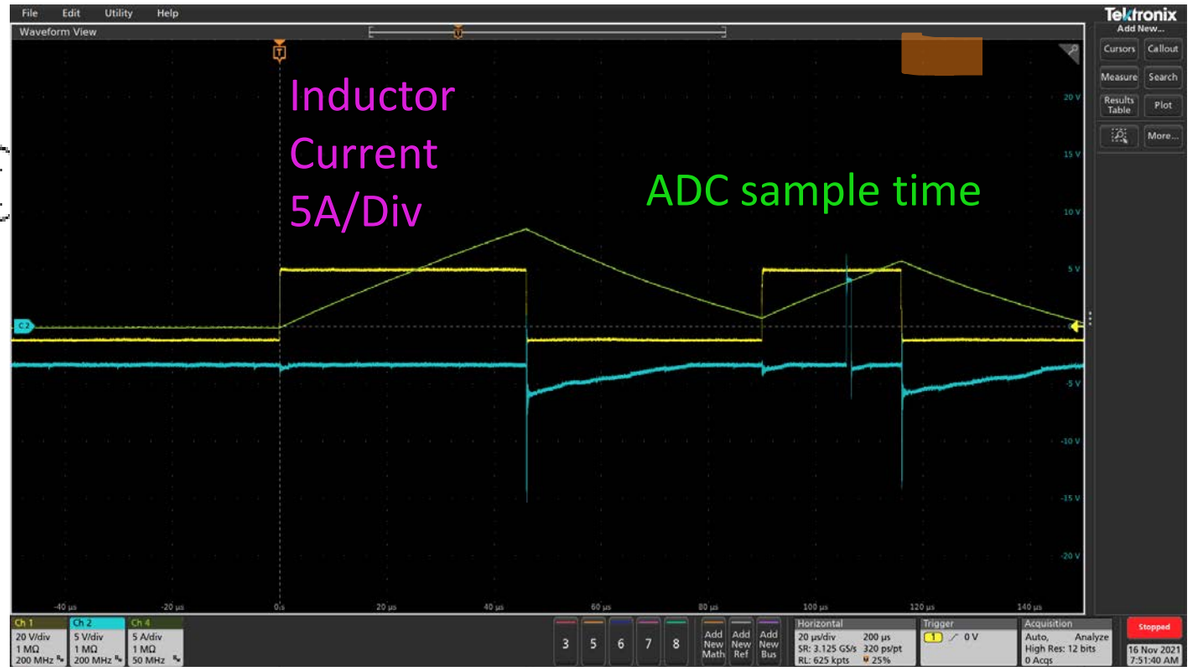
3. Intelligent gate driving, V_{on} and T measurement, over current protection

Novel Ron online monitoring scheme

V_{on} measurement utilizing the same DESAT over current protection circuit

ADC sample and hold to obtain V_M





$$V_{desat} = V_F + V_{zener} + R_{dson} * I$$

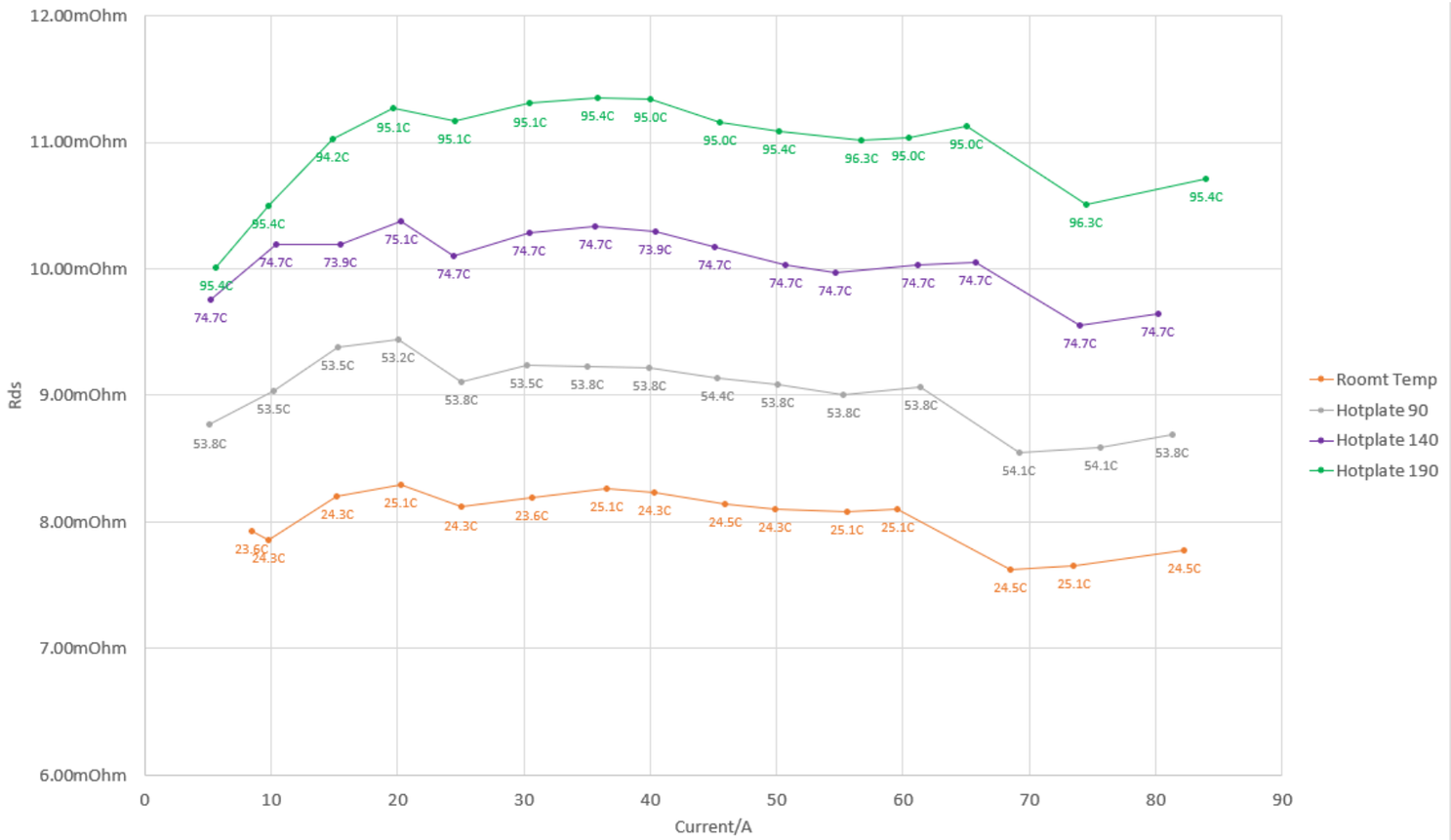
$$V_M = V_F - R_{ds} * I$$

12-bits ADC, 75nS Acquisition Window->1.566uS,
2 samples/per acquisition

Innovation Update

3. Intelligent gate driving, V_{on} and T measurement, over current protection

Online Monitoring Results Obtained through a DPT test



Device: UF3SC120009K4S
Hotplate temperature room, 90, 140, 190 °C.
Forward conduction, DPT, Fan Off

Rds calculated by: ADC voltage/scope current

Final implementation:
ADC voltage/ADC current temperature sensor provide T compensation info

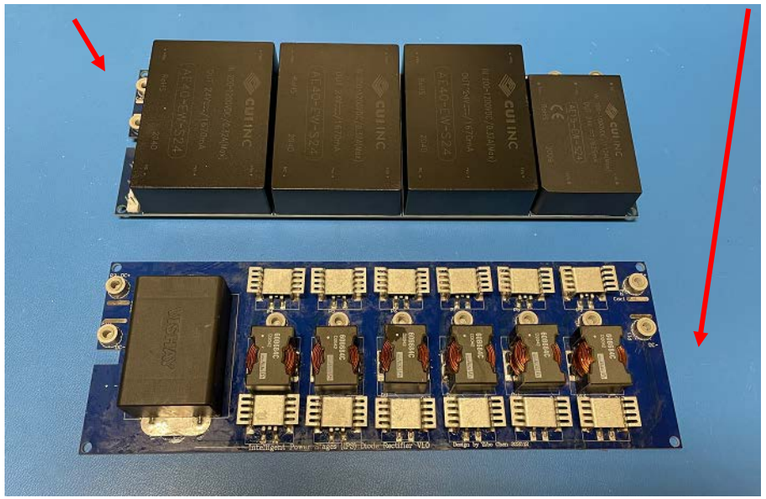
Innovation Update

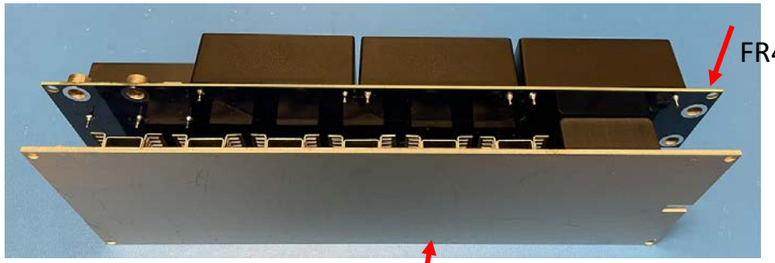
4. Self-contained auxiliary power supply unit

A natural air cooled 1kW auxiliary power supply is developed, which can start from both DC or AC side.

DC side Auxiliary power supply
262*90*27mm

AC side Diode bridge rectifier
262*90*27mm





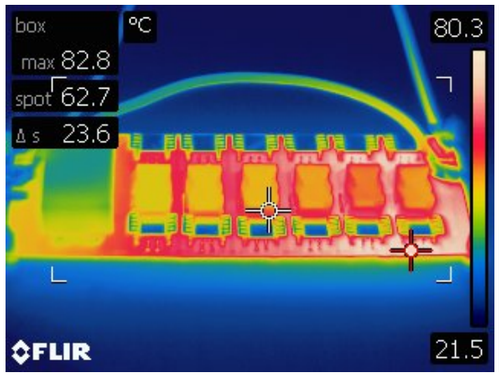
FR4 PCB

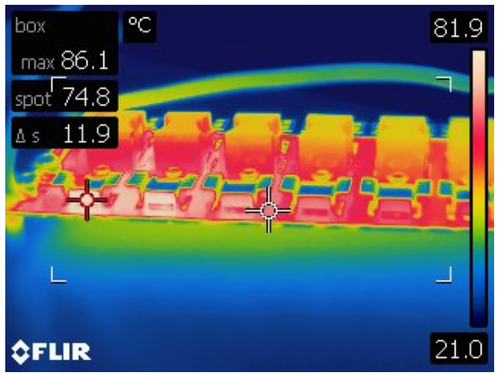
Aluminum based single layer PCB

An 1kW auxiliary power supply is built by aluminum-based PCB. The PCB itself serves as a heatsink without a bulky heatsink and fans. The design is verified by a thermal test, 3 A current is injected into each diode, temperature for each diode is 86.9°C in 23°C room temperature.

Input voltage(V)	Input current(A)	Current for each diode(A)	Total Input power(W)	Temperature
1.772	9	1.5	15.948	51.1
1.994	18	3	35.892	86.9

Natural cooling without fans for 20 min



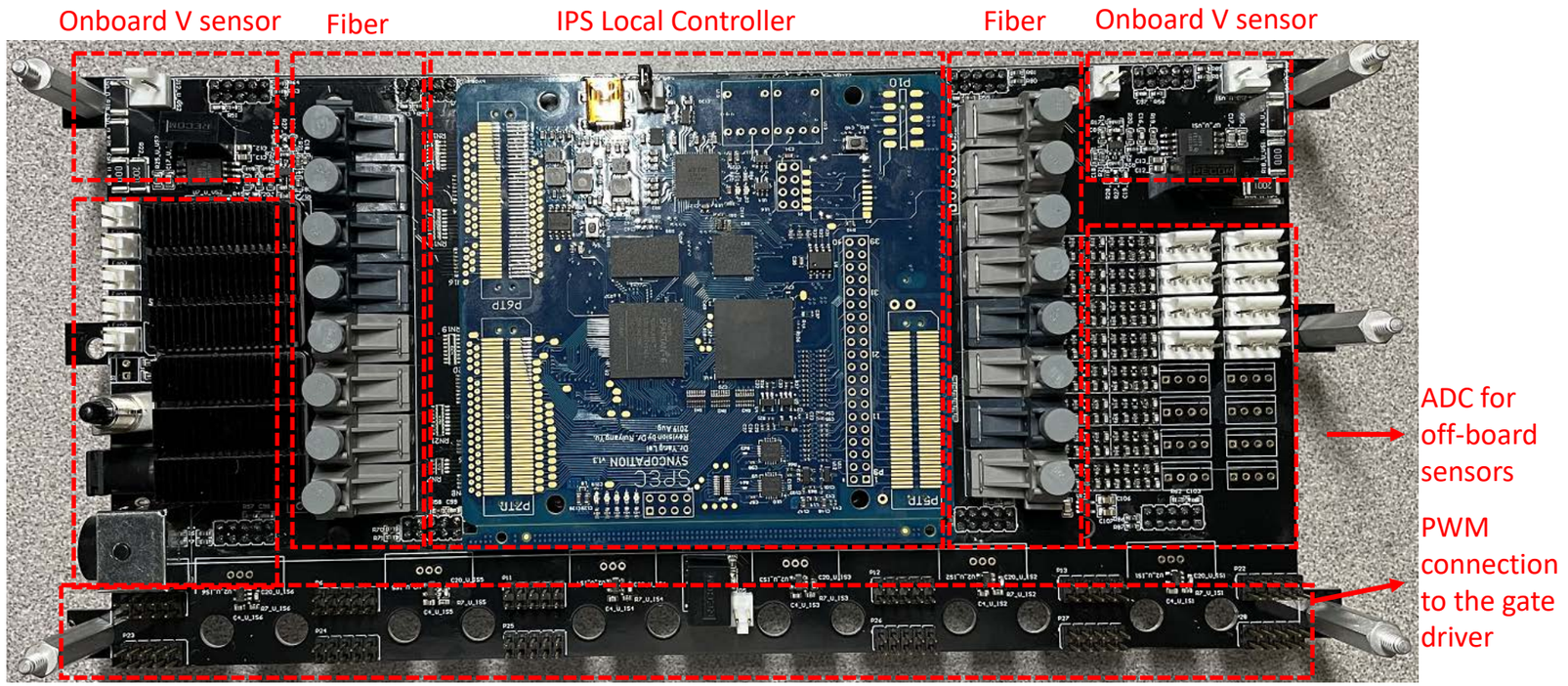


Innovation Update

5. Advanced DSP+FPGA controller and communication with SUPER

A DSP+FPGA controller is developed. Communication is verified between two DSP controller.

- 24 EPWM; 12 EN, 12 RDY (driver power supply), 12 Fault, 12 Temperature for gate drivers
- 2 onboard voltage sensors; 6 onboard current sensors; 16 off-board ADC (for current or voltage sensors)
- 3 SCI Receiver and 4 SCI Transmitter (Fiber); 5 IO Receiver and 4 IO Transmitter (Fiber)
- Communication with SUPER controller verified

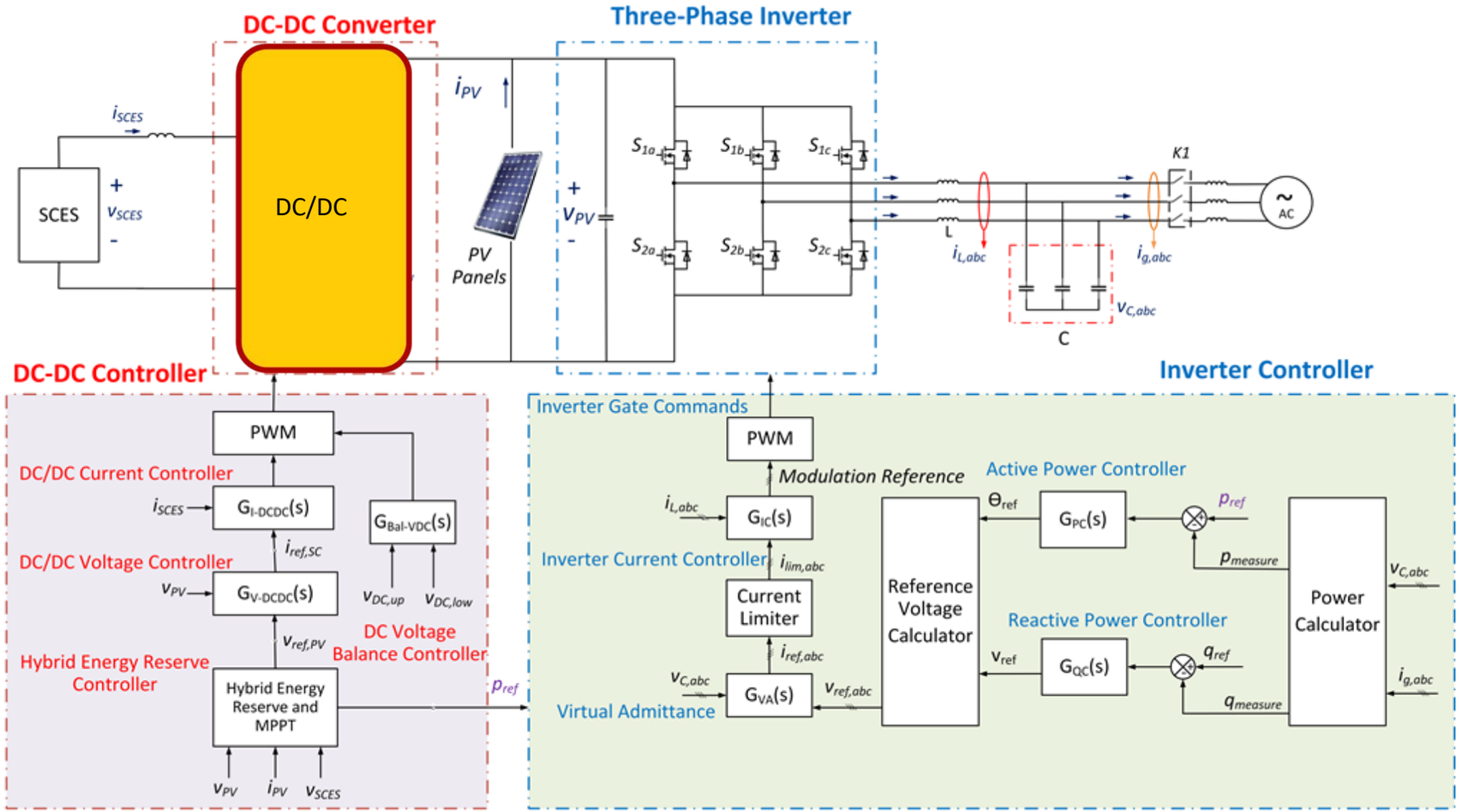


Innovation Update

6. Advanced grid functions (Black start, LVRT, inertia support, PV intermittence smoothing)

Grid forming/Voltage source close loop framework has been developed for PV + storage system using IPS

Battery
Or
Supercap
Or
Fuel cell

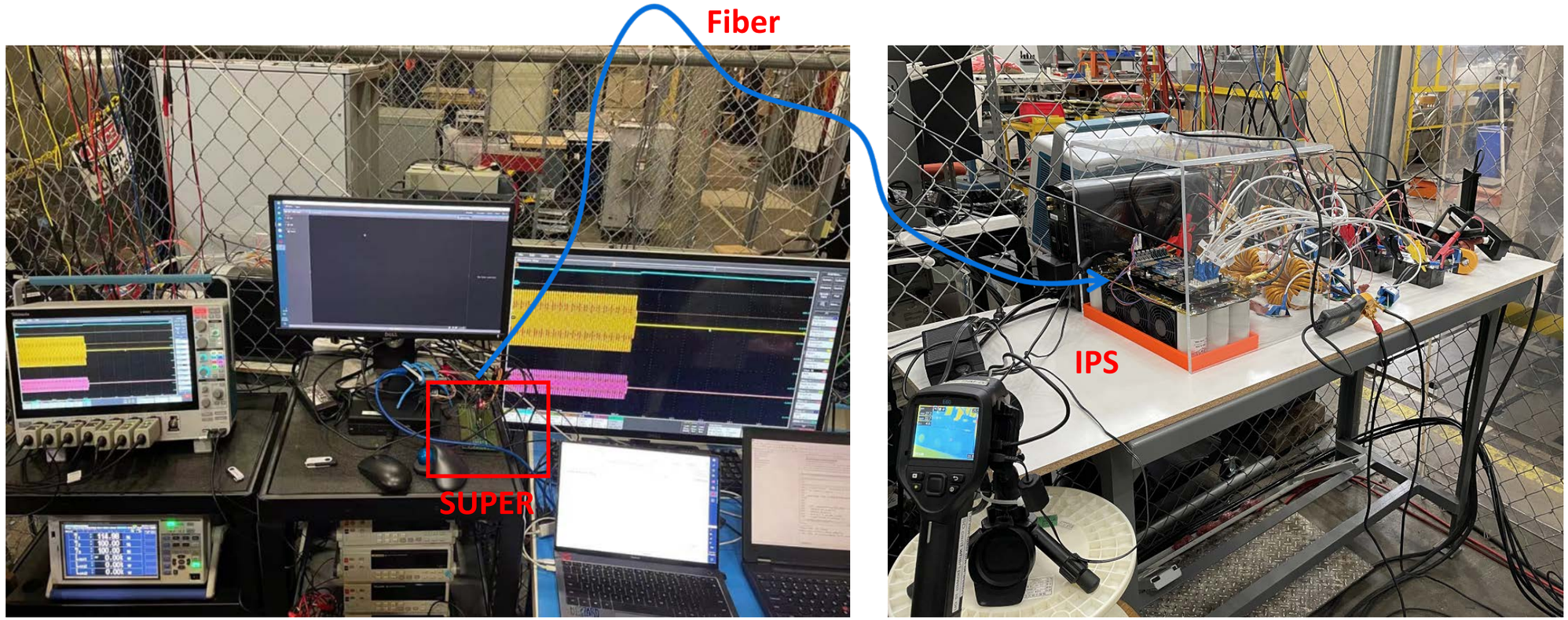


Innovation Update

IPS system level verification: SUPER communication is verified

Test setup

Close loop DC/AC test with SUPER + IPS via communication



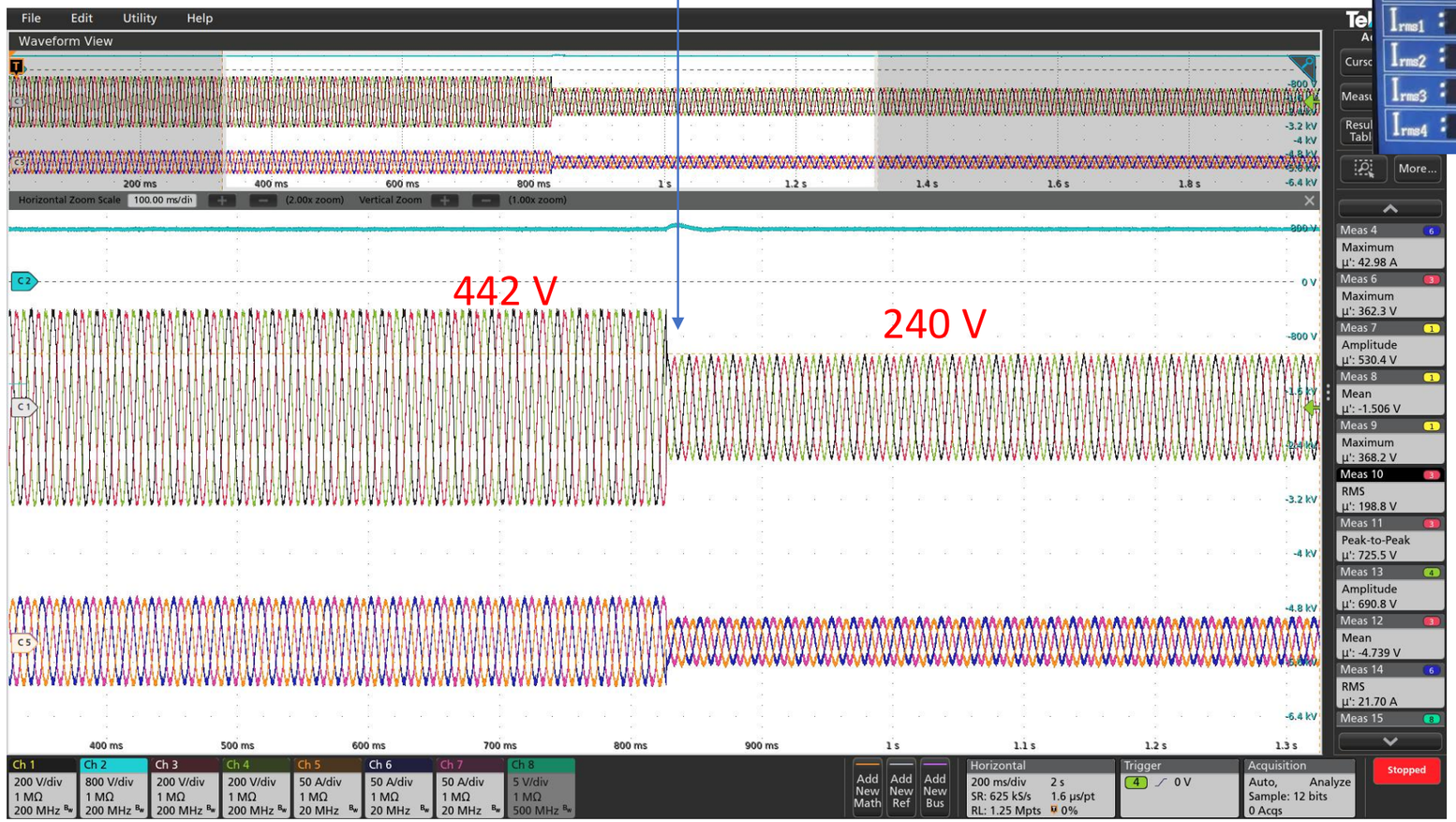
Innovation Update

IPS system level verification

DC/AC close test with SUPER + IPS via communication

AC output voltage step change, 442VAC to 240VAC, 21kW

SUPER send modulation index to IPS by optic fiber



Innovation Update

IPS system level verification

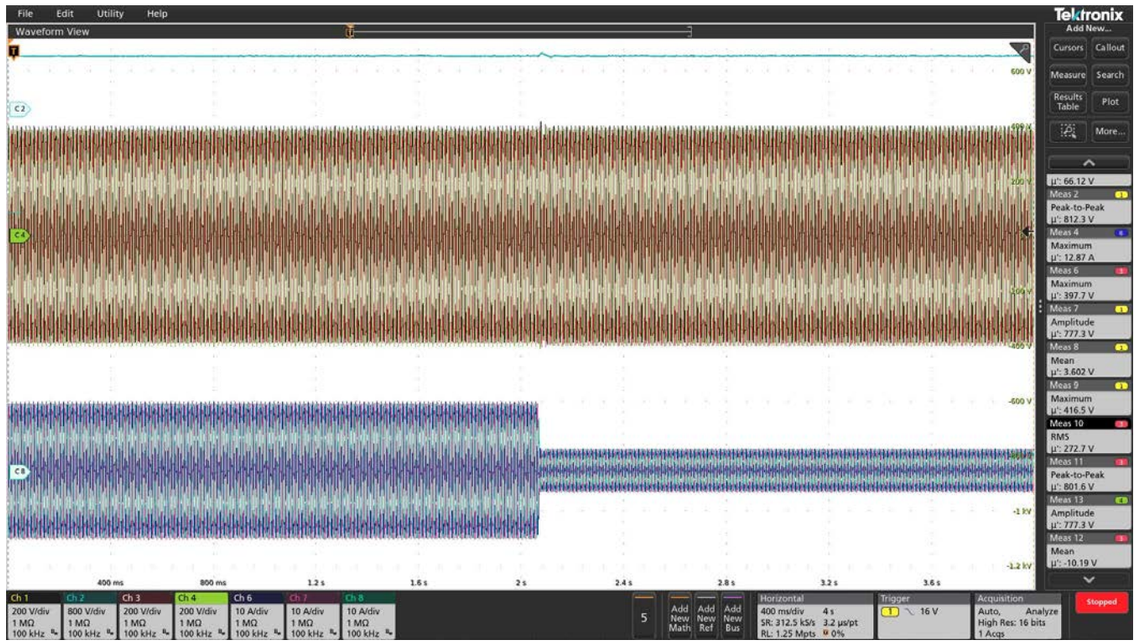
Close loop DC/AC test with SUPER + IPS via communication

Load step change, 7kW to 2kW, with resistive load bank

Vdc

Vac

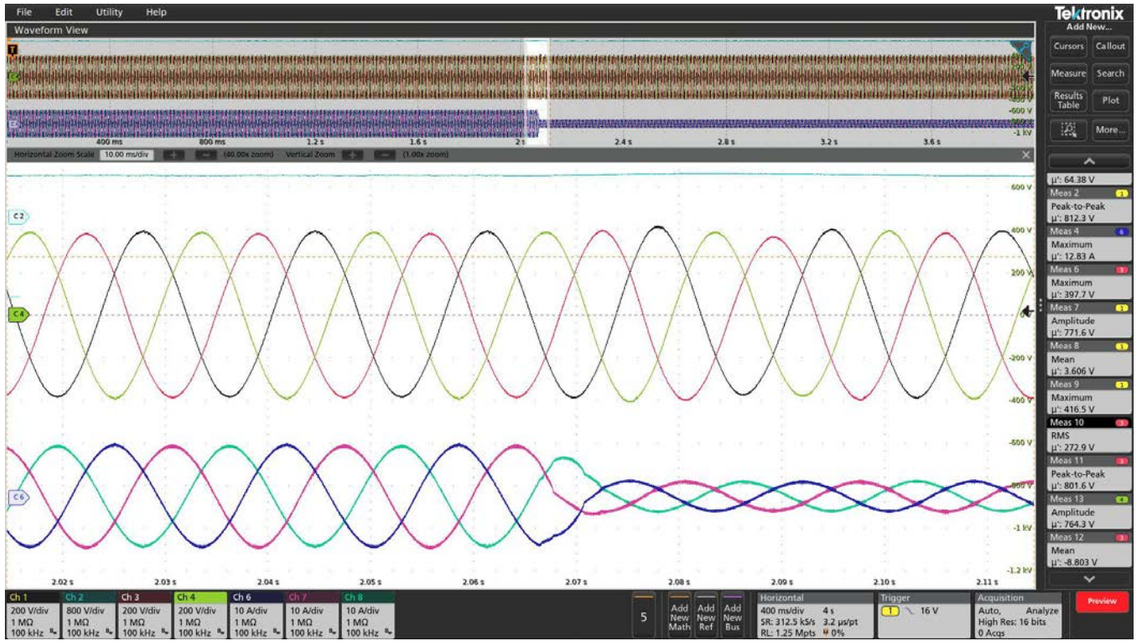
I



Vdc

Vac

I

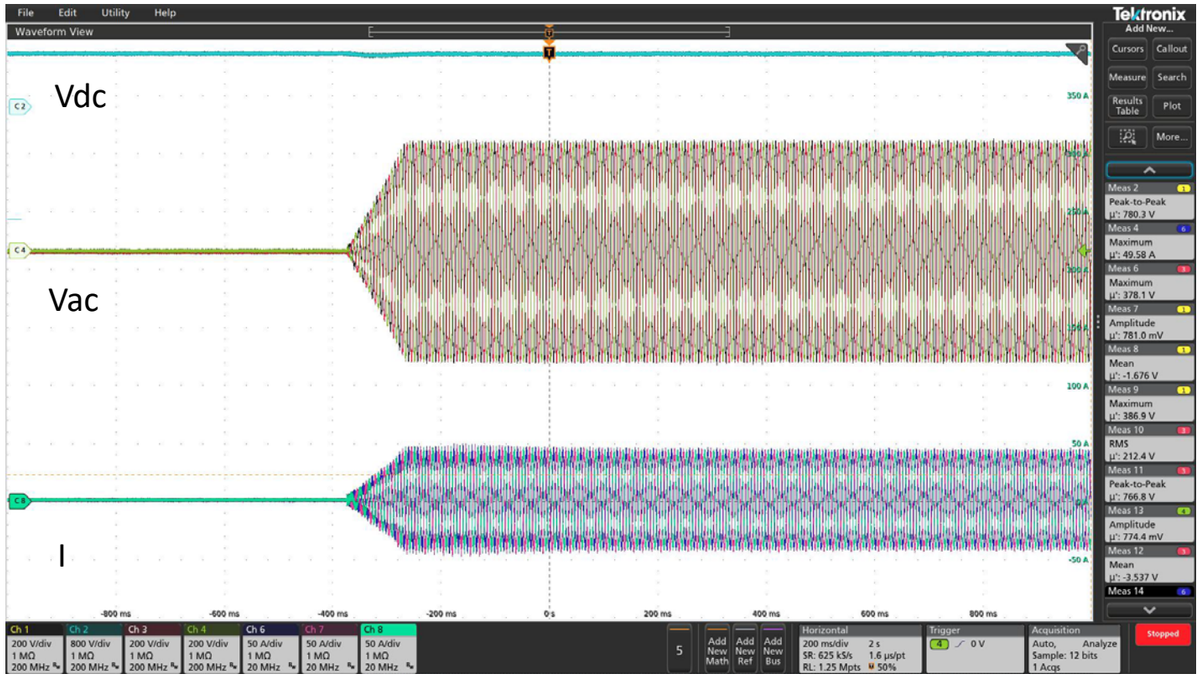


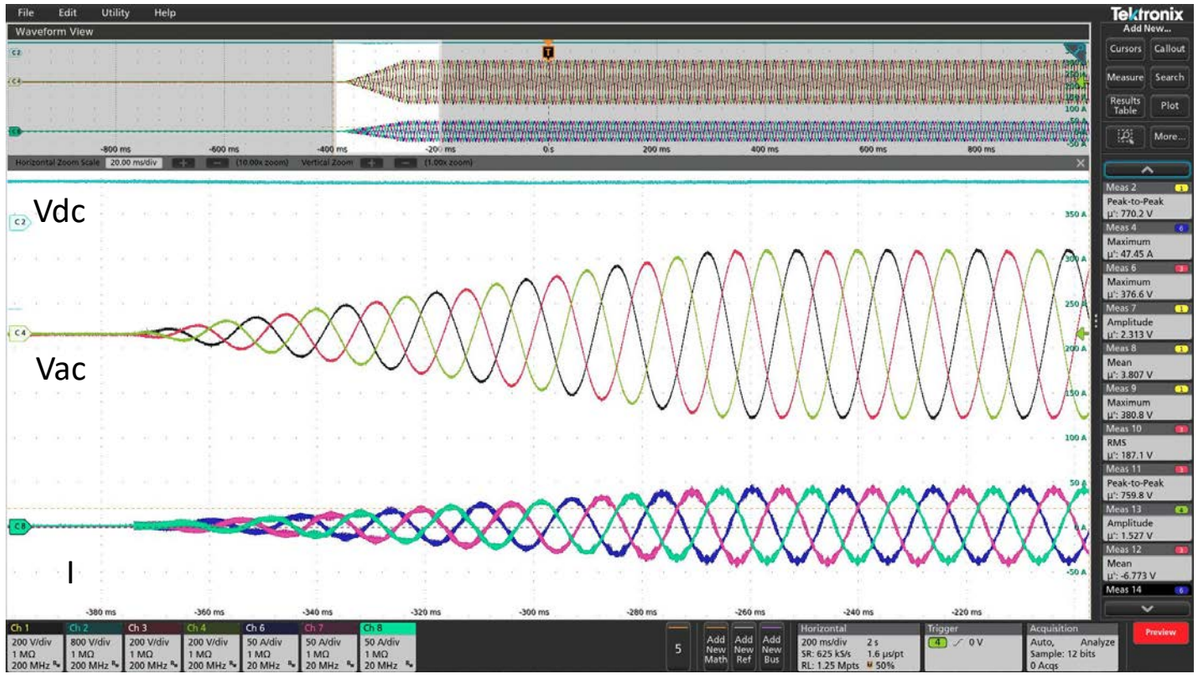
Innovation Update

IPS system level verification

Close loop DC/AC test with SUPER + IPS: Black start/Soft Start

Black start up with 25kW load, 800VDC, 480VAC

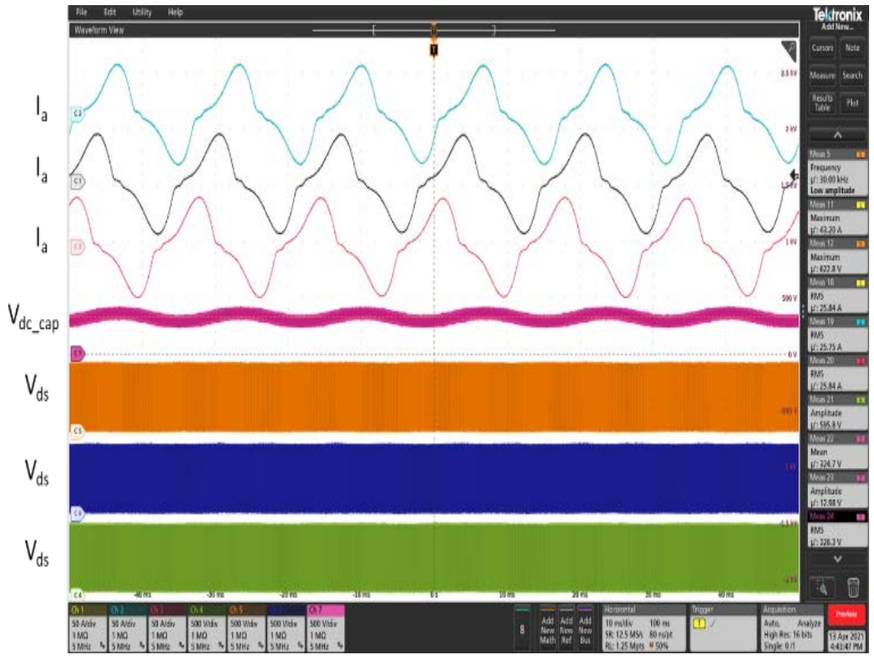




Innovation Update

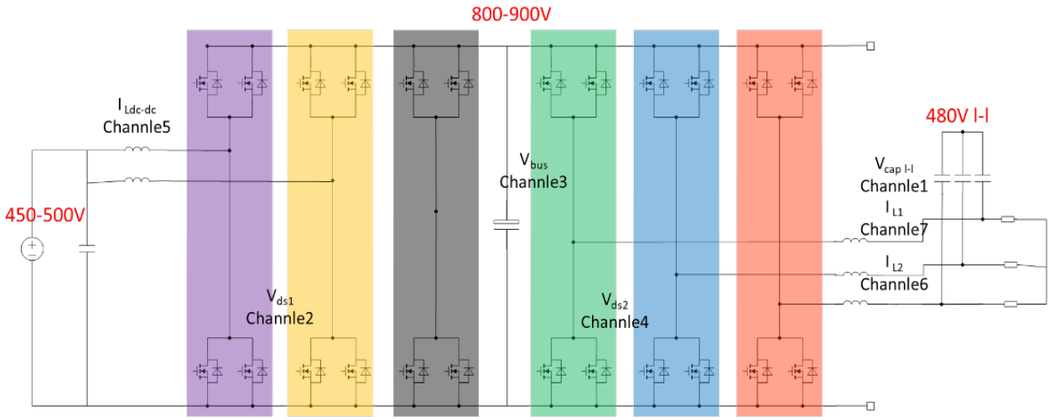
IPS system level verification: Efficiency verification

1. Back-to-Back Circulating test



Inverter circulating test with 600V DC bus: Loss=144W, Power = 14.8kW, efficiency=99%

2. Two stage DC/DC + DC/AC test

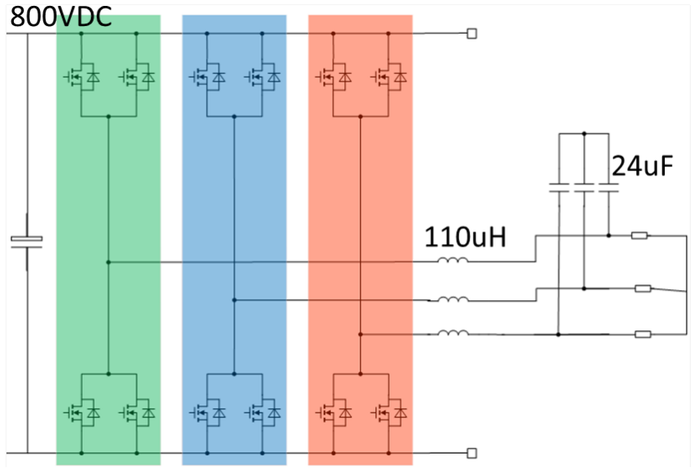


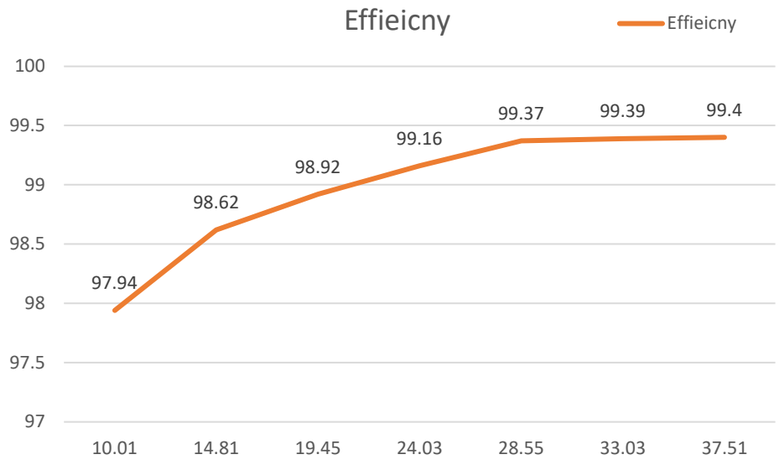
97.97% at 27 kW

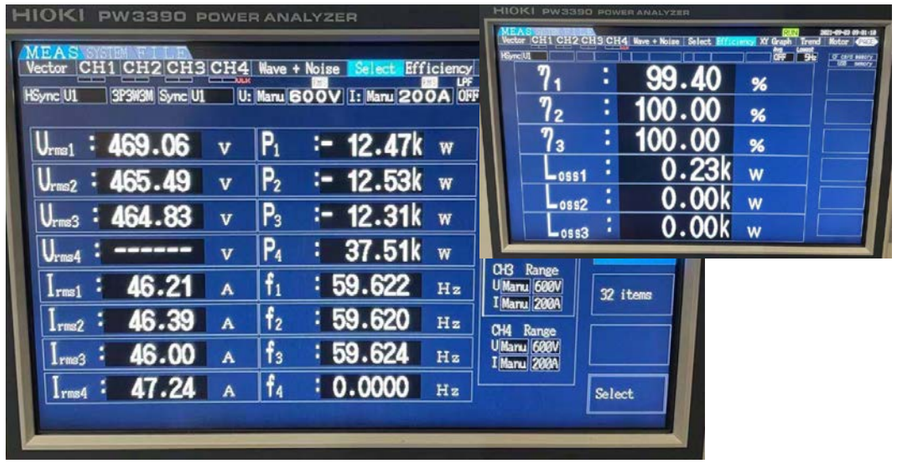
Innovation Update

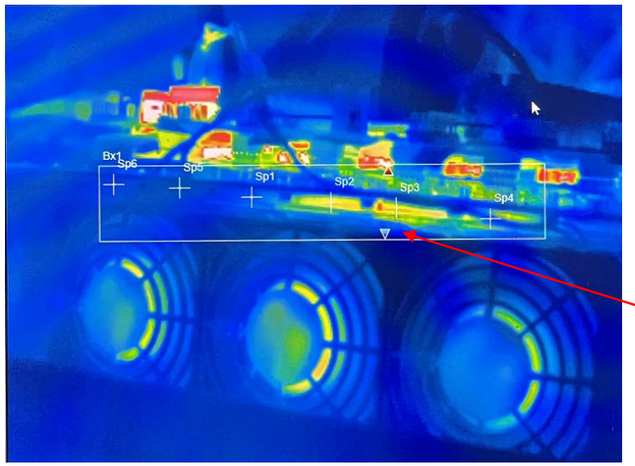
IPS system level verification: Efficiency verification

3. Close loop single stage DC/AC test, 99.4% efficiency demonstrated at 37kW









1-2 mins

32.5°C

Innovation Update

- Milestone update

  UT team has met the milestone for BP1 and BP2 Q1, additional tests are on-going.

BP1 Milestone	Description	Status
Q1	IPS specification finalized	Yes
Q2	SiC power module designed and fabricated	Yes
Q3	Alpha IPS Prototype fabricated	Yes
Q4: Power Stage Full Power Test	>50 kW Demonstration of all components of IPS	Yes. To 40kW with 99.4% single stage efficiency
BP2 Milestone		
Q5: Alpha Shipped to ORNL	IPS prototype-1 with functional power stage	Underway
Q6: Beta IPS shipped to ORNL	IPS prototype-2 with all IPS features and functions	
Q7: Grid functionality demonstration	IPS prototype -1 tested in grid connected mode and with advanced features with PF=1 and PF=0 operation.	
Q8: Demonstration of Beta at ORNL	Support ORNL to successfully demonstrate IPS prototype at ORNL	

Innovation Update

- Summarize the risks and mitigation strategy

  Very long lead time for some components especially on the DSP+FPGA controller, because of global IC shortage.

  Various delay caused by COVID

  Facility and space limitational at UT for high power test

- Future work

  Additional testing's at higher power level is on going. ‘

  Revising and implementing an improved SiC IPS to meet the deliverable needs to ORNL.

Impact/Commercialization

IMPACT/COMMERCIALIZATION STATUS

- Potentially offering industry and national labs a very high power density (44 kW/L if counting only the power stage) and high efficiency yet cost effective SiC IPS for various applications
- Project is still ongoing and commercialization opportunities will be explored

IP STATUS

Development is still underway and at the moment no invention has been filed.

PUBLICATIONS

1. Z. Chen, H. S. Rizi, C. Chen, P. Liu, R. Yu and A. Q. Huang, "An 800V/300 kW, 44 kW/L Air-Cooled SiC Power Electronics Building Block (PEBB)," IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society, 2021, pp. 1-6.

THANK YOU

This project was supported by the Department of Energy (DOE) - Office of Electricity's (OE), Transformer Resilience and Advanced Components (TRAC) program led by the program manager Andre Pereira & Oak Ridge National Laboratory (ORNL)

U.S. DEPARTMENT OF ENERGY | OFFICE OF ELECTRICITY

Acronyms

IPS: Intelligent Power Stage

SiC: Silicon Carbide

FPGA: Field Programmable Gate Array

DSP: Digital Signal Processor

DESAT: Desaturation

OC: Overcurrent

Video/Picture(Optional)

Use this slide if you plan on using a video